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Specification

(54) Title of Invention: THIN FILM TRANSISTOR ELEMENT

(57) Summary

[Problem to be solved] To offer a forward staggered type thin film transistor element which enables light-off current reduction, while maintaining good on-characteristic without using a shielding film.

[Solution] In a forward staggered type thin film transistor element which is used as a switching element of a pixel electrode of an active matrix liquid crystal display, wherein a source electrode 11 and a drain electrode 12, a silicon film 13 forming an active layer, a silicon nitride film 14 which is a gate insulating film, and a gate electrode 17 are laminated and formed one by one on a transparent insulating substrate 10 and either the source electrode 11 or the drain electrode 12 is connected to a pixel electrode, a fine crystalline silicon film which is formed by plasma CVD method formed by using mixed gas system as a raw material to which diborane is added in a concentration range of 5 to 300 ppm to monosilane is used as the silicon film 13.

[What is claimed]

[Claim 1] In a forward staggered type thin film transistor element which is used as a switching element of a pixel electrode of an active matrix liquid crystal display and in which a source electrode and a drain electrode, a silicon film forming an active layer, a gate insulating film, and a gate electrode are laminated and formed one by one on a transparent insulating substrate and either said source electrode or said drain electrode is connected to said pixel electrode,

wherein a fine crystalline silicon film which is formed by plasma CVD method formed by using mixed gas system as a raw material to which diborane is added in a concentration

range of 5 to 300 ppm to monosilane is used as said silicon film.

[Claim 2] A thin film transistor element of claim 1 wherein said fine crystalline silicon film is formed in layers all over below said gate electrode through a gate insulating film.

[Claim 3] A thin film transistor element of claim 1 wherein said fine crystalline silicon film is formed into island-shape connected to said source electrode and said drain electrode.

[Detailed Description of the Invention]

[0001]

[Field of the invention] The present invention relates to a thin film transistor element, especially to a forward staggered type thin film transistor element used in an active matrix liquid crystal display.

[0002]

[Prior art] Recently, an active matrix type liquid crystal display wherein a thin film transistor (TFT) in which a hydrogenated amorphous silicon film is used as an active layer is used as a switching element of each displaying pixel has been mass-produced. Especially, with the prevalence of a notebook type personal computer, the demand for liquid crystal display is increased rapidly, accordingly, the improvement of productivity are requested.

[0003] Figure 5 is a cross sectional view of a forward staggered type thin film transistor element used as a switching element of a pixel of a liquid crystal display by the conventional technology. In the Figure, 51 is a source electrode, 52 is a drain electrode, 53 is an amorphous silicon film, 54 is a gate insulating film, 56 is an n^+ silicon layer, 57 is a gate electrode, 58 is a shielding layer, and 59 is a transparent insulating film. In the forward staggered type thin film transistor, compared with an inversely staggered type one, the improvement of productivity can be realized by reducing the number of masks in manufacturing steps. In the forward staggered structure, because the gate electrode 57 exists above the amorphous silicon film 53 of an active layer, a back light beam irradiated from the back side of the transparent insulating substrate 50 of a glass substrate which exists below is incident directly on the amorphous silicon layer 53 so that carriers are produced in the amorphous silicon layer 53 and light-off current of a leak current is generated, consequently, the display quality is deteriorated by

discharging a connected pixel electrode. As shown in this figure, in order to prevent this phenomenon, an incident light to a back channel side is shielded by providing the shielding film 58 of metal and the like at below the amorphous silicon film 53 through the transparent insulating film 59 to keep light-off current low. Consequently, the practical off resistance is obtained, and good holding characteristic is ensured.

[0004] Also recently, as shown in Figure 6, for the purpose of further simplifying processes for forming a thin film transistor, in the forward staggered type thin film transistor, development of the technology which makes it possible to omit a shielding film by lowering the photo sensitivity by forming an amorphous silicon layer into a thin film.

[0005] Figure 6 is a cross sectional view of a forward staggered type thin film transistor element in which an amorphous silicon layer by the conventional technology is made to be thin, in the Figure, 61 is a source electrode, 62 is a drain electrode, 63 is an amorphous silicon film, 64 is a gate insulating film, 66 is an n^+ silicon layer, and 67 is a gate electrode.

[0006] For example, on pp 957-958 of ASIA DISPLAY' 95, it is reported that the cross talk can be restrained without using a shielding film in a liquid crystal display for a laptop computer by forming an amorphous silicon layer into a thin film up to about 200 Å.

[0007] As a forming technology of a fine crystalline silicon film in which diborane is doped, an example is reported on pp 25-30 of Materials Research Society Symposium Proceedings Vol. 366 in 1994. It is described that high mobility can be realized by using a fine crystalline silicon film in an active layer of a reverse staggered type thin film transistor.

[0008]

[Problems to be solved by the Invention] In the conventional forward staggered type thin film transistor, values of about 300 to 1000 Å are used as a thickness of an amorphous silicon film of an active layer. If the thickness of this amorphous silicon film is made to be thin to about not more than 200 Å, as the report mentioned above, the photo sensitivity of the thin film transistor is lowered so that it is able to make light-off current lower without using a shielding film, however, a problem that the on-current is lowered at the same time is caused. A phenomenon that the on-current is lowered accompanied

by making amorphous silicon layer thin like this is generally known. Besides, in case of using a fine crystalline silicon film in an active layer of a thin film transistor, there is a problem that how to compensate the defect of donor and to make it intrinsic. In future, accompanied by making liquid crystal display large area and high definition further, high performance is requested in a thin film transistor, and the maintenance of high on-current at making the active layer thin, that is to say, a thin film transistor with high mobility is necessary.

[0009] Therefore, it is necessary to develop a new forward staggered type thin film transistor device technology which enables light-off current reduction by using a material with higher electron mobility than that of the conventional amorphous silicon film as an active layer, while maintaining good on-characteristic at the manufacturing step of active layer into thin film.

[0010] The present invention has a purpose to offer a forward staggered type thin film transistor element which enables light-off current reduction, while maintaining good on-characteristic without using a shielding film.

[0011]

[Means for resolving problems] A thin film transistor element of the present invention is that; in a forward staggered type thin film transistor element which is used as a switching element of a pixel electrode of an active matrix liquid crystal display and wherein a source electrode and a drain electrode, a silicon film forming an active layer, a gate insulating film, and a gate electrode are laminated and formed one by one on a transparent insulating substrate and either the source electrode or the drain electrode is connected to a pixel electrode, a fine crystalline silicon film which is formed by plasma CVD method formed by using mixed gas system as a raw material to which diborane is added in a concentration range of 5 to 300 ppm to monosilane is used as the silicon film.

[0012] A fine crystalline silicon film can be formed in layers all over below a gate electrode through a gate insulating film, and the fine crystalline silicon film can be formed to island-shape connected to a source electrode and a drain electrode.

[0013] The fine crystalline silicon film formed in this way has the electron mobility higher than the conventional amorphous silicon film so that light-off current is reduced at making the film thin, while maintaining good on-characteristic.

[0014]

[Embodiment mode] Hereafter, an embodiment mode of the present invention is explained referring to Figures. Figure 1 is a cross sectional view of a forward staggered type thin film transistor element which is used as a switching element of a pixel of a liquid crystal display of the first embodiment mode of the present invention, Figure 2 is a cross sectional view showing manufacturing processes of a thin film transistor element of the first embodiment mode, (a) shows a condition of forming a source and a drain electrodes, (b) is a condition of piling up phosphorus on a electrode, (c) is a condition of piling up an active layer, a gate insulating film and a gate electrode, (d) is a condition of patterning a gate electrode, a gate insulating film and an active layer. Number 11 is a source electrode, 12 is a drain electrode, 13 is a fine crystalline silicon film, 14 is a silicon nitride film of a gate insulating layer, 16 is an n^+ silicon layer, and 17 is a gate electrode in the Figure.

[0015] Manufacturing processes of the first embodiment mode of the present invention is explained in detail with Figure 2 (a) to (d). As shown in Figure 2 (a), a source electrode 11 and a drain electrode 12 are formed by patterning a transparent conductive film ITO film which is formed on a glass substrate 10 of an insulating substrate to the preferable shape. Subsequently, as shown in Figure 2 (b), phosphorus 15 is piled up by phosphine plasma processing with plasma CVD method. Furthermore as shown in Figure 2 (c), a fine crystalline silicon film 13 to be an active layer and a silicon nitride film 14 to be a gate insulating film are piled up in order by plasma CVD method, continuously metal for a gate electrode 17 is piled up by sputtering. When the fine crystalline silicon film 13 is piled, a silicon layer 16 to be n-type is formed on an interface between the source electrode 11/the drain electrode 12 and the fine crystalline silicon film 13 by diffusion of phosphorus. Subsequently, as shown in Figure 2 (d), the metal for the gate electrode 17, the silicon nitride film 14, the fine crystalline silicon film 13 and the silicon layer 16 to be n-type are patterned into the preferable shape, consequently the thin film transistor element of the first embodiment mode of the present invention shown in Figure 1 is accomplished. In the present structure, the gate electrode 17, the silicon nitride film 14, the fine crystalline silicon film 13 and the silicon layer 16 to be n-type are processed by etching with the same mask, accordingly the fine crystalline silicon film 13 exists in

layers all over below the gate electrode 17. Besides, by processing with the same mask, high throughput of process and reduction in costs can be realized.

[0016] Figure 3 is a cross sectional view showing manufacturing processes of a thin film transistor element of the second embodiment mode of the present invention, (a) shows a condition of forming a source and a drain electrodes, (b) is a condition of piling up phosphorus on a electrode, (c) is a condition of piling up an active layer and a gate insulating film and patterning them to an island-shape, (d) is a condition of piling up a protective film and a gate electrode, and patterning them, number 31 is a source electrode, 32 is a drain electrode, 33 is a fine crystalline silicon film, 34 is a silicon nitride film of a gate insulating layer, 36 is an n^+ silicon layer, and 37 is a gate electrode in the Figure.

[0017] Manufacturing processes of the second embodiment mode of the present invention is explained in detail with Figure 3 (a) to (d). As shown in Figure 3 (a), a source electrode 31 and a drain electrode 32 are formed by patterning a transparent conductive film ITO film which is formed on a glass substrate 30 of an insulating substrate into a preferable shape. Subsequently, as shown in Figure 3 (b), phosphorus 35 is piled up by phosphine plasma processing with plasma CVD method. Furthermore, as shown in Figure 3 (c), a fine crystalline silicon film 33 to be an active layer and a silicon nitride film 34 to be a gate insulating film are piled up in order by plasma CVD method, and these films are patterned into the preferable island-shape only at the portion of the thin film transistor element. When the fine crystalline silicon film 33 is piled up, a silicon layer 36 to be n-type is formed at an interface with the source electrode 31, the drain electrode 32, and the fine crystalline silicon film 33 by diffusion of phosphorus. Furthermore, a silicon nitride film 38 is formed by plasma CVD method as a protective film, continuously metal for a gate electrode 37 is piled up by sputtering and patterned, as shown in Figure 3 (d), the thin film transistor element of the second embodiment mode of the present invention is accomplished. In the present structure, though the number of processes is increased compared with the first embodiment mode, the fine crystalline silicon film 33 is to be an island-shape so that the leak current between the gate electrode and the fine crystalline silicon film through the gate insulating film can be restrained much lower.

[0018] Normally, a fine crystalline silicon film has been formed by using high hydrogen diluted monosilane as raw material gas to which hydrogen that have ten times or more flow rate more than that of monosilane was mixed. However, when the activation energy of electric conductivity of the fine crystalline silicon films formed under such conditions was measured, any of them had the value about 0.2 eV, accordingly it was thought to be n-type. Therefore, in case of using a fine crystalline silicon film as an active layer of a thin film transistor, it is necessary to compensate the defect of donor by doping of a very small quantity and to make it intrinsic. And then in the present invention, a fine crystalline silicon film to be intrinsic is formed by using high hydrogen diluted monosilane and diborane mixed gas system as a raw material to which a very small quantity of diborane in a concentration range of 5 to 300 ppm to monosilane is doped. Accordingly, a fine crystalline silicon film having the same extent of activation energy as the intrinsic silicon about 0.5 to 0.6 eV can be formed.

[0019] Next, an embodiment based on an embodiment mode of the present invention is explained referring to Figures.

[0020]

[Embodiment] The first embodiment of the first embodiment mode of the present invention is explained. A forward staggered type thin film transistor is formed as the first embodiment of the first embodiment mode of the present invention in order of processes shown in Figure 2 (a) to (d). A transparent conductive film ITO film is formed to a thickness of 500 Å by sputtering. Phosphine plasma processing is performed by using argon base 0.5 % phosphine gas. A thickness of a fine crystalline silicon film of an active layer is 100 Å, and that of a silicon nitride film of a gate insulating film is 4000 Å. The forming conditions of the fine crystalline silicon film are as follows; a raw material gas of monosilane 15 SCCM, hydrogen base 20 ppm diborane 40 SCCM, hydrogen 1000 SCCM is used and the gas pressure is 150 Pa, the introducing electricity density is 0.04 Wcm^{-2}, and the substrate temperature is 300 ℃. The activation energy of the fine crystalline silicon film formed under these conditions is about 0.6 eV. The characteristic of gate voltage/drain current when light is irradiated of the forward staggered type thin film transistor in this embodiment is shown in Figure 4. Figure 4 is a graph showing the characteristic of gate voltage/drain current in light-irradiated

condition of the first embodiment of the first embodiment mode of the present invention, and also the characteristic of a thin film transistor in which the conventional amorphous silicon film of 100 Å is used for activation is shown for comparison. A shielding film is not provided and light is incident on the active layer in either thin film transistor. As understood from this Figure, in the thin film transistor by the present invention, enough lower light-off current can be realized without using a shielding film, and the good characteristic is maintained in on-region, consequently the practical value which can be applied to a liquid crystal display with the field effect mobility of about 0.4 $cm^2V^{-1}s^{-1}$ is obtained.

[0021] The second embodiment of the first embodiment mode of the present invention is explained. It is the same way as the first embodiment except the forming condition of a fine crystalline silicon film of an active layer. The forming conditions of the fine crystalline silicon film are as follows; a raw material gas of monosilane 15 SCCM, hydrogen base 20 ppm diborane 150 SCCM, hydrogen 1000 SCCM is used and the gas pressure is 150 Pa, the introducing electricity density is 0.02 Wcm^{-2}, and the substrate temperature is 300 ℃. The activation energy of the fine crystalline silicon film formed under these conditions is also about 0.6 eV. In case of reducing the introducing electricity density, the decomposition efficiency of diborane is lowered, accordingly, it is necessary to increase the supply of diborane gas compared with the case of the first embodiment. In the thin film transistor in which the fine crystalline silicon film like this is used, the same good characteristic as the first embodiment can be obtained.

[0022] Next, an embodiment of the second embodiment mode of the present invention is explained. A forward staggered type thin film transistor is formed as an embodiment of the second embodiment mode of the present invention in order of processes shown in Figure 3 (a) to (d). A transparent conductive film ITO film is formed to a thickness of 500 Å by sputtering. Phosphine plasma processing is performed by using argon base 0.5 % phosphine gas. Subsequently a fine crystalline silicon film of an active layer is formed to a thickness of 100 Å, and a silicon nitride film of a gate insulating film is formed to a thickness of 500 Å by plasma CVD method. The forming conditions of the fine crystalline silicon film are as follows; a raw material gas of monosilane 15 SCCM, hydrogen base 20 ppm diborane 40 SCCM, hydrogen 1000 SCCM is used and the gas

pressure is 150 Pa, the introducing electricity density is 0.04 Wcm^{-2}, and the substrate temperature is 300 ℃. The activation energy of the fine crystalline silicon film formed under these conditions is about 0.6 eV. Continuously, these fine crystalline silicon film and silicon nitride film are patterned into the preferable island shape only on the thin film transistor element portion. Subsequently, a silicon nitride film is formed to a thickness of 3500 Å all over the substrate by plasma CVD method. Finally, Cr is piled up to a thickness of 1000 Å by sputtering as a material for a gate electrode and is patterned into the preferable shape, consequently a thin film transistor element is accomplished.

[0023] As a material for a source and drain electrode or a gate electrode, metal such as Cr, Al, Mo, etc. can be used. Regarding the diluting quantity of hydrogen when an active layer is deposited, the fine crystallization can be realized by diluting with hydrogen having the flow rate not less than ten times more than that of monosilane. Regarding the quantity of adding diborane, in case of under 5 ppm, even if the introducing electricity density is increased enough, the defect of donor cannot be compensated sufficiently. Besides, in case of over 300 ppm, conversely the property of p-type is shown, accordingly the adding quantity in range of 5 ppm to 300 ppm to monosilane is suitable.

[0024]

[Effect of the present invention] By using the present invention explained above, reduction of light-off current can be realized without using a shielding film, while maintaining on-characteristic of a forward staggered type thin film transistor in the practical level. By the present invention, simplification of processes for forming high performance forward staggered type thin film transistor and reduction in costs can be realized, consequently, advantages are brought that that large area and high definition TFT-LCD can be produced at a low price.

[A brief explanation of Figures]

[Figure 1] Figure 1 is a cross sectional view of a forward staggered type thin film transistor element which is used as a switching element of a pixel of a liquid crystal display of the first embodiment mode of the present invention.

[Figure 2] A cross sectional view showing manufacturing processes of a thin film transistor element of the first embodiment mode. (a) shows a condition of forming a

source and a drain electrodes. (b) shows a condition of piling up phosphorus on a electrode. (c) shows a condition of piling up an active layer, a gate insulating film and a gate electrode. (d) shows a condition of patterning a gate electrode, a gate insulating film and an active layer.

[Figure 3] A cross sectional view showing manufacturing processes of a thin film transistor element of the second embodiment mode of the present invention. (a) shows a condition of forming a source and a drain electrodes. (b) shows a condition of piling up phosphorus on a electrode. (c) shows a condition of piling up an active layer, a gate insulating film and patterning them to an island-shape. (d) shows a condition of piling up a protective film and a gate electrode, and patterning them.

[Figure 4] A graph of the characteristic of gate voltage/drain current in light irradiated condition of the first embodiment of the first embodiment mode of the present invention.

[Figure 5] A cross sectional view of a forward staggered type thin film transistor element which is used as a switching element of a pixel of a liquid crystal display by the conventional technology.

[Figure 6] A cross sectional view of a forward staggered type thin film transistor element in which an amorphous silicon layer by the conventional technology is made to be thin.

[An explanation of marks]

11, 31, 51, 61	source electrode
12, 32, 52, 62	drain electrode
13, 33	fine crystalline silicon film
14, 34	silicon nitride film
16, 36, 56, 66	n^+ silicon layer
17, 37, 57, 67	gate electrode
53, 63	amorphous silicon film
54, 64	gate insulating film
58	shielding film
59	transparent insulating film